REMARKS

This is in response to the Office Action dated April 3, 2008. Claims 1-4, 7-10 and 19-23 are pending. Claims 1-4, 7-10 and 19-23 stand rejected in the outstanding office Action.

The rejection of claims 1, 20 and 23 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Tomita et al. (US 5,191,405) in view of Iwamoto (US 2003/0017654) is respectfully traversed.

Tomita generally discloses a stacked semiconductor device (Fig. 1h), comprising multiple semiconductor chips 1, 6, 15 and 23. The semiconductor chips are connected electrically with through electrodes 9, 22 and 27. Each electrode is formed within the area of an electrode pad, e.g., 4. The Examiner acknowledged that Tomita does not teach "at least one type of the through electrodes is a non-contact through electrode of electrically conductive material that is not electrically connected to any electrode pad of the semiconductor chip in which the non-contact through electrode is formed". He then turned to Iwamoto for the missing limitation.

Iwamoto discloses a method for forming a tape BGA type semiconductor package 170, as shown in Fig. 3. First, a semiconductor chip 100 is formed having a plurality of bump electrodes 3 along the periphery, each bump electrode formed on a pad 2 (Fig. 1). In the middle area 50 of the semiconductor chip 100, a supporting member 4 is formed ([0047]). The material of the supporting member 4 may be the same as that of the bump electrodes 3 ([0049]). Subsequently, the semiconductor chip 100 is affixed to a tape substrate 5 (Fig. 2). By thermal compression, each electrode 3 comes into contact with a corresponding land electrode 6 of the tape substrate ([0050]). Finally, the area between the semiconductor chip 100 and the tape substrate 5 is filled with resin 7 ([0053]). The tape BGA type semiconductor package 170 is then connected to the assemble substrate 9 via external land electrodes 6a (Fig. 4, [0057]).

The purpose of the supporting member 4 in Iwamoto is the following. When a semiconductor chip, like the one shown in Fig. 20 (i.e., missing the supporting member) is fixed on the tape substrate 5 (Fig. 21), the influence of heat or pressure during the thermal compression affects the tape substrate 5, resulting in deformation at several points, e.g., see Fig. 27, [0006]-[0010]. In this case, the gaps may not be filled with the resin material 7, or even if there are no gaps, the thickness of the resin material becomes uneven ([0011]). Therefore, a supporting member 4 is used for "planarizing the tape substrate 5 when the semiconductor chip 100 is mounted on the tape substrate 5", see [0048]. The Examiner identified supporting member 4 (or 4d in Fig. 16) as the claimed "non-contact through electrode".

However, from the above, it is clear that supporting member 4 is not an electrode. Instead, it is a structural member that is used to ensure that the tape substrate 5 remains planar after the thermal compression process. This is why the structural member 4 is not in contact with any electrodes on the tape substrate 5, unlike electrodes 3, each of which is in contact with a corresponding land electrode 6 on the tape substrate. In one embodiment, supporting member 4 is in contact with adhesive resin material 11 (Fig. 11 and [0094]-[0095]).

In addition, supporting member 4 is not formed in a region within an electrode pad. In Fig. 1 of Iwamoto, electrode pads are labeled "2". Iwamoto does not teach that the supporting members 4 are formed on electrode pads. Therefore, Iwamoto fails to teach "multiple electrically conductive through electrodes formed in a region within the electrode pads, wherein at least one type of the through electrodes is a non-contact through electrode".

Moreover, it would not have been obvious to combine Tomita and Iwamoto. Whereas, Tomita's device comprises a stacked semiconductor device having multiple semiconductor chips vertically stacked and connected via through electrodes, Iwamoto's device comprises a single

semiconductor chip, without any need for through electrodes. The tape substrate 5 is not a semiconductor chip having active elements ([0050]). One would not look into Iwamoto, teaching the use of a structural supporting element supporting the connection between a single semiconductor chip and a tape substrate, for modifying the type of the through electrodes used in the chip-stack device of Tomita.

Regarding claim 23, Fig. 5 in Iwamoto, cited by the Examiner, does not show "at least two of the electrically conductive through electrodes formed in a region within the same electrode pad", said electrodes not being in direct electrical contact. As discussed above, supporting members 4 are not electrodes, and moreover, are not formed within an area of an electrode pad.

For the above reasons, claims 1, 20 and 23 are allowable.

It is respectfully requested that the rejection of claims 2-4, 7-10, 19, 21 and 22, each of which being dependent from independent claim 1 or 20, be also withdrawn.

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

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